Specification

For

LCD Module

2004A

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1.0 INTRODUCTION

This USER'S MANUAL is introduced the outside dimensions, optical characteristics, electrical characteristics, interface, controller commands, etc. of the custom design LCD module.

1.1 FEATURE

(1) Display mode: STN POSITIVE, TRANSFLECTIVE, YELLOW-GREEN COLOR

(2) Display format: 20 characters X 4 line

(3) Driving method: 1/16 Duty, 1/5 Bias

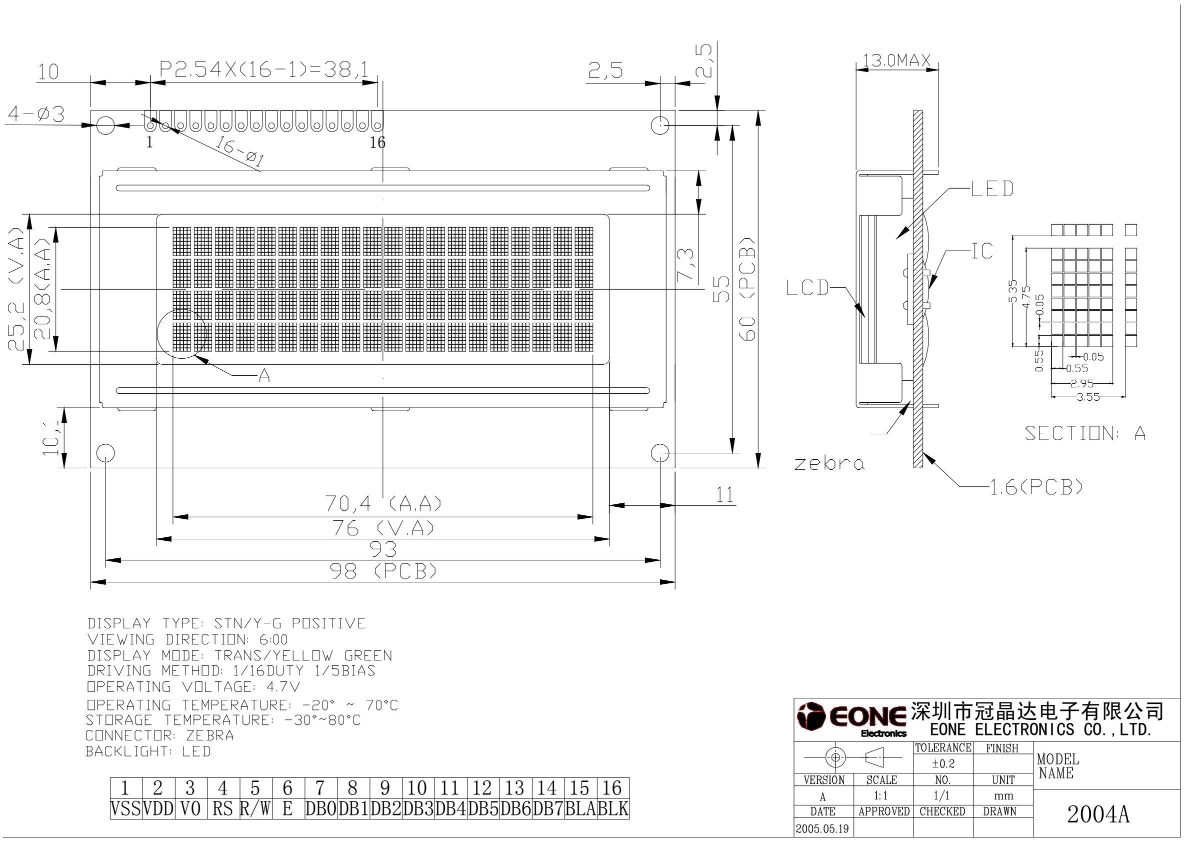
(4) Viewing direction: 6 o'clock

(5) Control IC: SPLC780D

(6) Interface Input Data : 4-Bits or 8-Bits interface available

(7) Back light: LED (Yellow-Green)

2.0 DIMENSION DIAGRAM



3.0 MECHANICAL SPECIFICATIONS

ITEM	STANDARD VALUE	UNIT
DOTS	5X8	characters -
DOT SIZE	0.55X0.55	mm
DOT PITCH	0.60X0.60	mm
MODULE DIMENSION	98.0(W) × 60.0(H) × 1.6(T)	mm
EFFECTIVE DISPLAY AREA	84.0(W) × 31.0(H)MIN	mm

4.0 MAX STANDARD VALUE

ITEM	SYMBOL	MIN.	TYPE	MAX	UNIT
OPERATING TEMPERATURE	Top	-10	25	60	℃
STORAGE TEMPERATURE	Tst	-20	/	70	℃
INPUT VOLTAGE	VI	VSS	/	VDD	V
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	-0.3	/	7.0	V
SUPPLY VOLTAGE FOR LCD	VDD-V0	VDD-10.0	/	VDD+0.3	V

5.0 ELECTRICAL CHARACTERISTICS

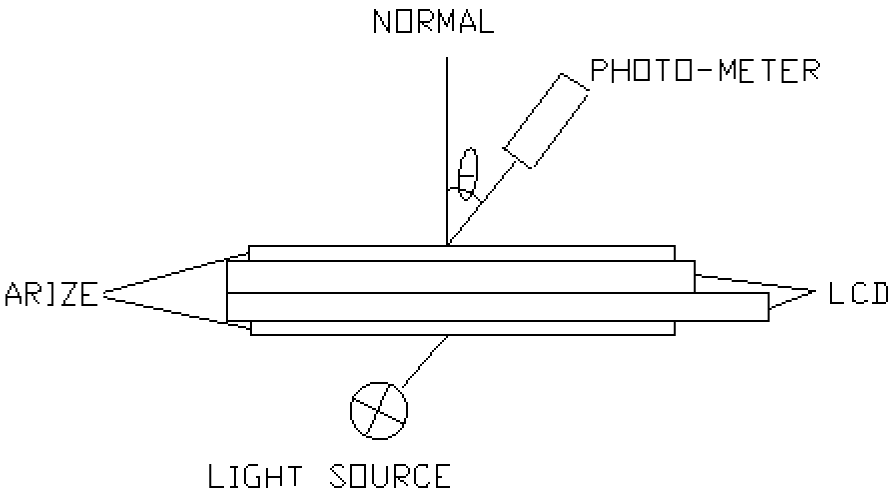
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT

SUPPLY VOLTAGE FOR LOGIC	V_{DD}-V_{SS}	Ta = 25 °C	2.7	5.0	5.5	V
SUPPLY VOLTAGE FOR LCD	V_{DD}-V_O (V_{OP})	Ta = 25 °C	3.0	5.0	10.0	V
INPUT HIGH VOL.	V_{IH}	Ta = 25 °C	0.7VDD	-	VDD	V
INPUT LOW VOL.	V_{IL}	Ta = 25 °C	-0.3	-	0.6	V
OUTPUT HIGH VOL.	V_{OH}	Ta = 25 °C	0.75VDD	-	-	V
OUTPUT LOW VOL.	V_{OL}	Ta = 25 °C	-	-	0.2VDD	V
SUPPLY CURRENT	IDD	VDD = 3.0V	-	0.1	0.25	mA

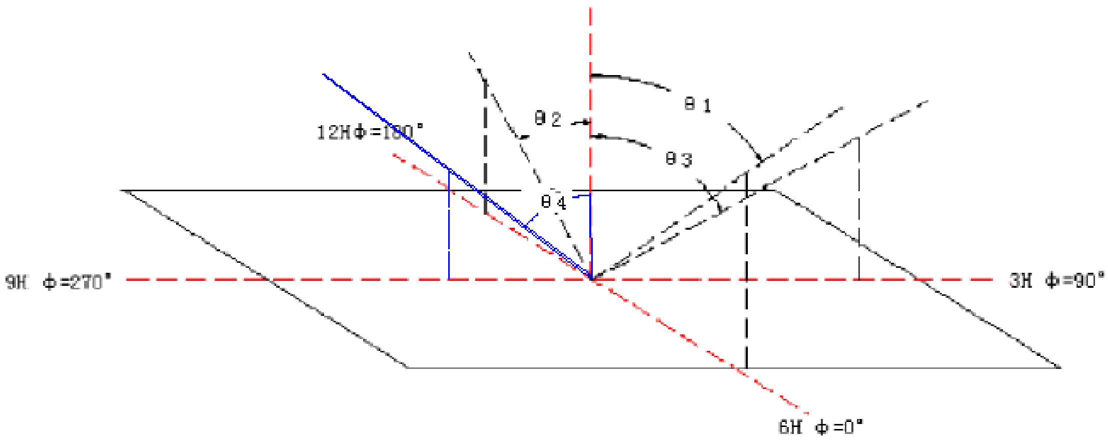
6.0 OPTICAL CHARACTERISTICS

No	Item		Symbol	Measurement temperature	MIN.	TYP.	MAX.	Unit
1	Contrast Ratio		Cr	25℃	2.60	3.17		
2	Response Time	Rise time	Tr	25℃	-	-	0.2	us
		Fall time	Tf	25℃	-	-	0.2	us
3	Viewing Angle	6H, Φ=0°	θ 1	25℃	55			Deg.
		12H, Φ=180	θ 2	25℃	0			Deg.
		Φ=90°	θ 3	25℃	45			Deg.
		Φ=270	θ 4	25℃	45			Deg.
4	Frame Frequency			25℃	190	270	350	Hz

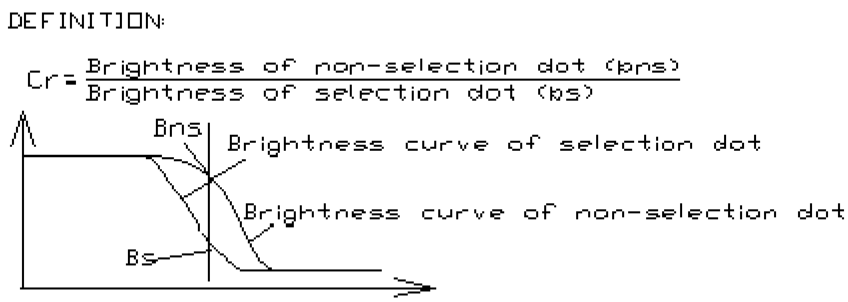
6.1 OPTICAL MEASUREMENT SYSTEM



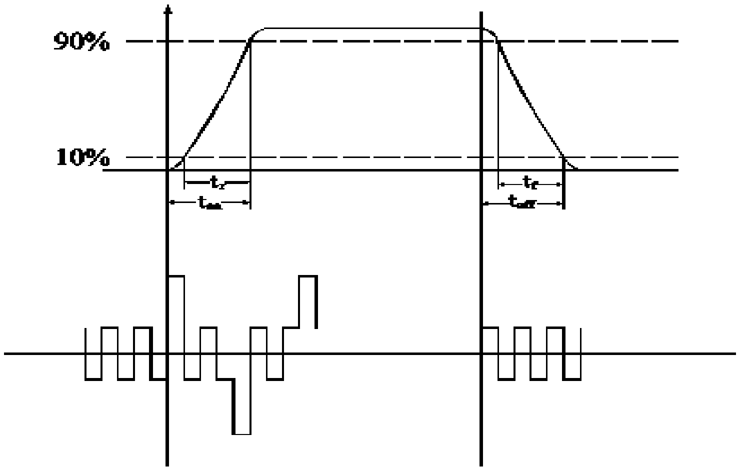
6.2 DEFINITION OF θ AND Φ



6.3 DEFINITION OF CONTRAST RATIO Cr



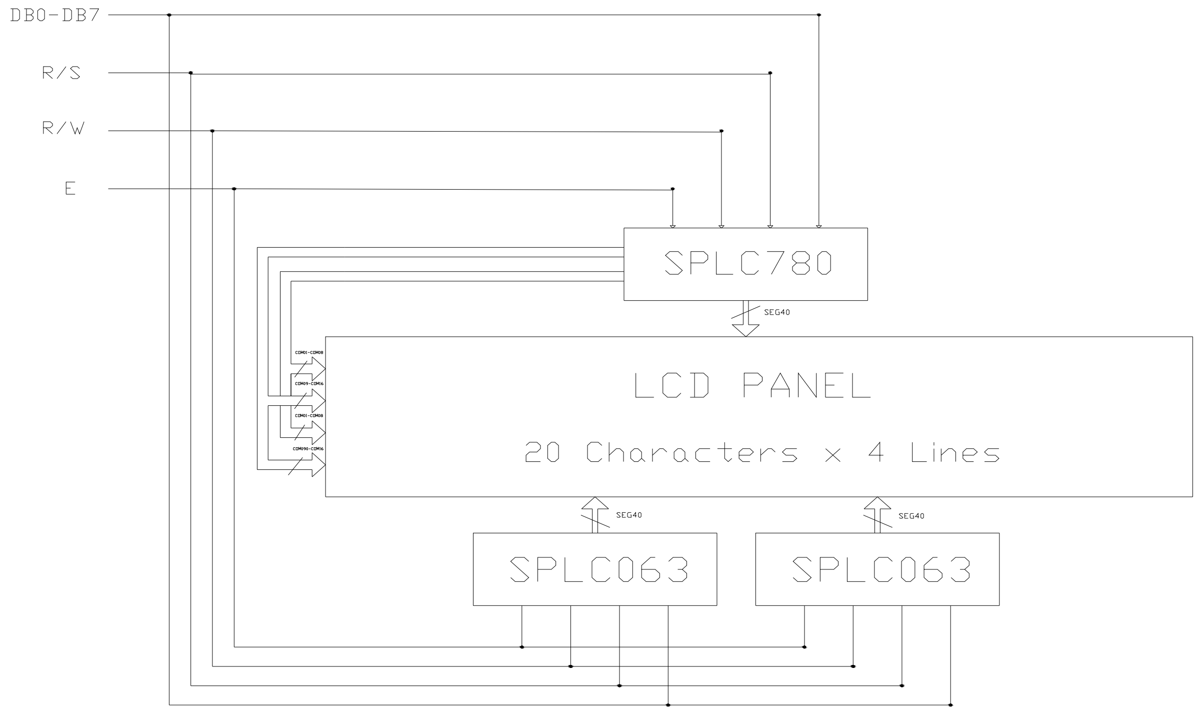
6.4 DEFINITION OF OPTICAL RESPONSE TIME



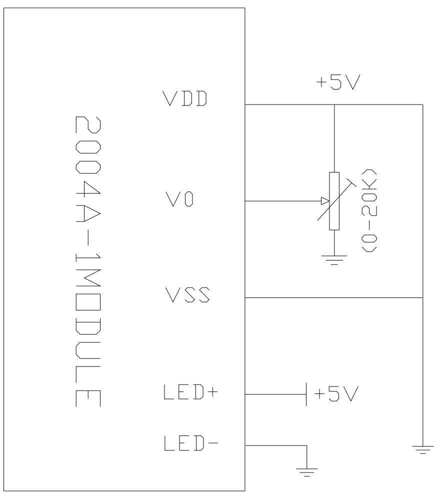
7.0 INTERFACE PIN FUNCTION DESCRIPTION

PIN NO	SYMBOL	FUNCTION
1	VSS	Power Ground
2	VDD	Power supply for logic circuit(+5V)
3	V0	For LCD drive voltage (variable)
4	RS(C/D)	H: Display Data, L:Display Instruction
5	R/W	H: Data Read (LCM to MPU) ; L: Data Write (MPU to LCM)
6	E	Enable signal. Write mode (R/W = L) data of DB<0:7> is latched at the falling edge of E. Read mode (R/W = H) DB<0:7> appears the reading data while E is at high level
7-14	DB0-DB7	Data bus. There state I/O common terminal.
15	A	Power for LED Backlight (+5V)
16	K	Power for LED Backlight (Ground)

8.0 BLOCK DIAGRAM



8.1 POWER SUPPLY BLOCK DIAGRAM



9.0 TIMING CHARACTERISTICS

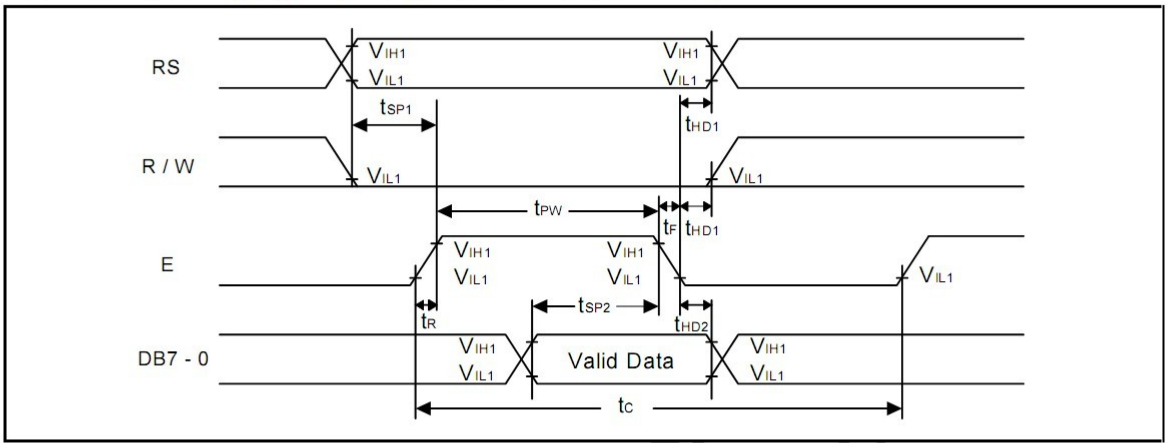
7.3.3. Write mode (Writing data from MPU to SPLC780D)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1000	-	-	ns	Pin E
E Pulse Width	t_{PW}	450	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	195	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

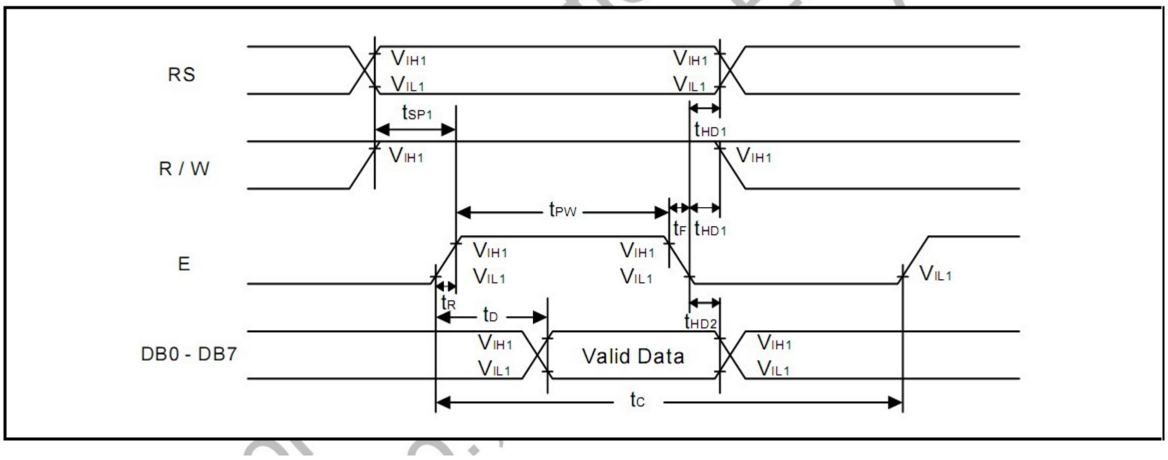
7.3.4. Read mode (Reading data from SPLC780D to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1000	-	-	ns	Pin E
E Pulse Width	t_W	450	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	360	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	5.0	-	-	ns	Pin DB0 - DB7

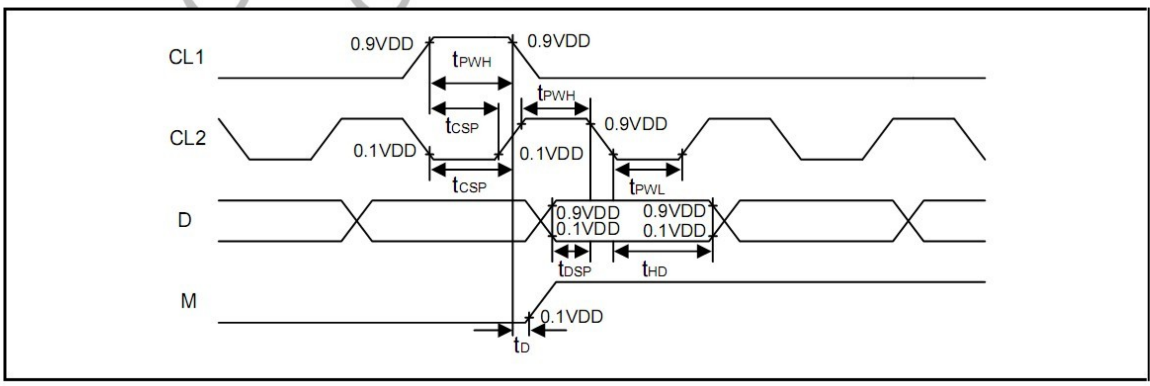
7.5.6. Write mode timing diagram (Writing Data from MPU to SPLC780D)



7.5.7. Read mode timing diagram (Reading Data from SPLC780D to MPU)



7.5.8. Interface mode with SPLC100A1 timing diagram



10.0 Display control instruction

The display control instructions control the internal state of the SPLC780D-01. Instruction is received from MPU to SPLC780D-01for the display control. The following table shows various instructions.

6.3. Instruction Table

Instruction	Instruction Code										Description	Execution time (Temp = 25℃)		
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Fosc= 190KHz	Fosc= 270KHz	Fosc= 350KHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	2.16ms	1.52ms	1.18ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	2.16ms	1.52ms	1.18ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display	53μs	38μs	29μs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor(C), and blinking of cursor(B) on/off control bit.	53μs	38μs	29μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	53μs	38μs	29μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5x10 dots/5x8 dots)	53μs	38μs	29μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	53μs	38μs	29μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	53μs	38μs	29μs
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.			
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	53μs	38μs	29μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	53μs	38μs	29μs

Note1: "--": don't care

Note2: In the operation condition under -20℃ ~ 75℃, the maximum execution time for majority of instruction sets is 100us, except two instructions, "Clear Display" and "Return Home", in which maximum execution time can take up to 4.1ms.

■ Instruction Description

● **Clear Display**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

● **Return Home**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	x

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

● **Entry Mode Set**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

➢ **I/D : Increment / decrement of DDRAM address (cursor or blink)**
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

➢ **S: Shift of entire display**
When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

- **Display ON/OFF**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

- **D : Display ON/OFF control bit**
  When D = "High", entire display is turned on.
  When D = "Low", display is turned off, but display data is remained in DDRAM.
- **C : Cursor ON/OFF control bit**
  When C = "High", cursor is turned on.
  When C = "Low", cursor is disappeared in current display, but I/D register remains its data.
- **B : Cursor Blink ON/OFF control bit**
  When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
  When B = "Low", blink is off.

- **Cursor or Display Shift**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	x	x

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Description	AC Value
L	L	Shift cursor to the left	AC=AC-1
L	H	Shift cursor to the right	AC=AC+1
H	L	Shift display to the left. Cursor follows the display shift	AC=AC
H	H	Shift display to the right. Cursor follows the display shift	AC=AC

- **Function Set**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	x	x

- **DL : Interface data length control bit**
  When DL = "High", it means 8-bit bus mode with MPU.
  When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
  When 4-bit bus mode, it needs to transfer 4-bit data by two times.
- **N : Display line number control bit**
  When N = "Low", it means 1-line display mode.
  When N = "High", 2-line display mode is set.
- **F : Display font type control bit**
  When F = "Low", it means 5 x 8 dots format display mode
  When F = "High", 5 x11 dots format display mode.

N	F	No. of Display Lines	Character Font	Duty Factor
L	L	1	5x8	1/8
L	H	1	5x11	1/11
H	x	2	5x8	1/16

- **Set CGRAM Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

- **Set DDRAM Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".

In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

- **Read Busy Flag and Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

When BF = "High", indicates that the internal operation is being processed.So during this time the next instruction cannot be accepted.

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

- **Write Data to CGRAM or DDRAM**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

- **Read Data from CGRAM or DDRAM**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

10. CHARACTER GENERATOR ROM

10.1. SPLC780D1 – 001A

